MONOBIT RECEIVER

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ABSTRACT

This paper presents a very simple digital receiver design which can cover approximately 1 GHz bandwidth and process two simultaneous signals. The design has the potential to be fabricated on a single chip.

I. INTRODUCTION

This digital receiver design uses a fast Fourier transform (FFT) to obtain frequencies on only two simultaneous signals. It has fine frequency resolution (capability to separate two close frequencies) and good frequency accuracy. The single signal and two signal spur free dynamic range should be rather high. The only deficiency in this design is that the instantaneous dynamic range (receiving a strong and a weak signal simultaneous) is low. Technical approach to design this receiver and experimental results will be presented. The performance of the monobit receiver will be compared with a conventional digital receiver. This receiver can be used to replace the existing instantaneous frequency measurement (IFM) receivers which can process only one signal.

II. TECHNICAL DISCUSSION

The design of this receiver can be divided into four areas. They are the radio frequency (RF) front end, the analog-to-digital converter (ADC), the FFT operation and the frequency selection logic. The receiver is shown in Figure 1. They will be discussed briefly in the following sections.

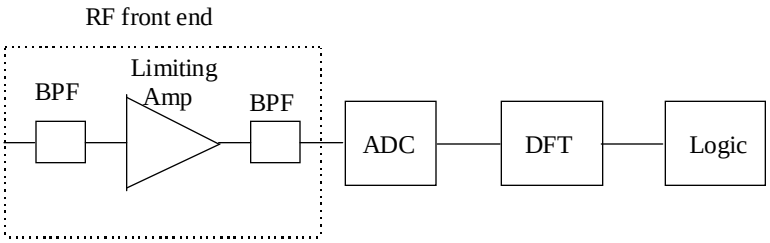

Figure 1. Four areas of monobit receiver

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A. RF front end: The RF front end will be similar to a conventional IFM receiver. The input signal will pass a bandpass filter followed by a limiting amplifier with 60 dBgain to amplify the input to a constant level. At the output of the limiting amplifier, another bandpass filter is used to limit the output spurs produced by the amplifier and also limit the out-of-band noise[1]. In this design, the filters have a passband from 1.375-2.375 GHz. This design will provide high single signal dynamic range. The two tone spur free dynamic range is also high because the receiver processes only two signals and the spurs will be neglected. The nonlinear characteristic of the limiting amplifier will cause capture effect which limits the instantaneous dynamic range.

B. ADC requirements: Because the signal from the limiting amplifier has a constant amplitude, a 2 bit ADC will be satisfactory. Experimental results showed that 2 bit ADC is better than 1 bit, but 3 or more bit ADCs show very little improvement, because of the limiting amplifier and the unique FFT design discussed in the next section. In order to cover 1 GHz bandwidth, the ADC should operate at about 2.5 GHz. The two lowest unambiguous ranges are from 0-1.25 and 1.25-2.5 GHz. A 1 GHz portion (1.375-2.375 GHz) from the second unambiguous frequency range is selected as the input bandwidth. The input frequency response of the ADC must be high enough to accommodate the input bandwidth of the receiver.

C. FFT design: This is the key component to the monobit design. The purpose is to eliminate multiplications and keep only adders in the discrete Fourier transform DFT chip design. The DFT can be written as[2,3]

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi kn}{N}} \qquad (1)$$

In this equation the result is obtained from the product of two functions: the input x(n) and the kernel function $e^{-\frac{j2\pi kn}{N}}$. If either one of these two functions is 1 bit (monobit), i.e. ±1, the operation requires only additions. With limited investigation, it appears that it is easier toimplement the monobit kernel function in hardware than the monobit input. The kernel function $e^{-\frac{j2\pi kn}{N}}$ is rounded to ±1 and ±j and this is then mapped to a time-decimated, radix-2 FFT algorithm. The FFT contains 256 points. Sampling at 2.5 GHz the total time is about 100 ns

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which can be considered as the minimum pulse width. The frequency cell is 9.8 (1250/128) MHz. In order to further simplify the design, the adders are limited to a maximum of 7 bits (6 bit amplitude and 1 bit sign). If the outputs from the adders are beyond 7 bits, they will be truncated to 7 bits.

D. Frequency selection logic: This is one of the most difficult designs in electronic warfare receivers with multiple signal capability. The goal is to select the correct input frequencies and avoid picking up spurious responses. Since the number of input signals is unknown, it is difficult to obtain the correct answer, especially if high instantaneous dynamic range is desired. In the monobit receiver design, the maximum number of signals to be processed is limited to two. Thus, the receiver is only required to determine between zero and two signals. In addition the instantaneous dynamic range of this receiver is low, because of the RF front end design and the 2 bit ADC. These two requirements simplify the logic frequency design significantly. One only needs to check the two highest peaks in the frequency domain to see whether they cross certain thresholds.

III. EXPERIMENTAL RESULTS

Since the RF limiting amplifier and 2 bit ADC are highly nonlinear, it is difficult to simulate the results accurately. An experimental set-up was used to evaluate the performance of the receiver. The experimental set-up is shown in Figure 2.

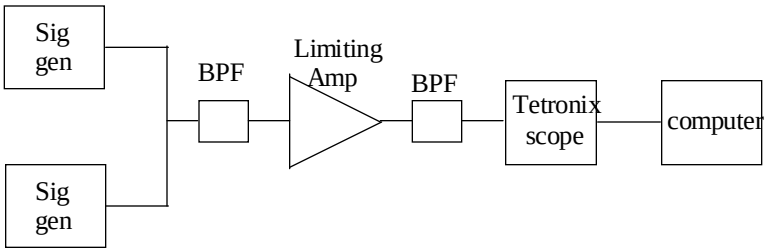

Figure 2. Experimental set-up

In this figure, the limiting amplifier has a gain of approximately 60 dB. The input bandwidth of this set-up was 1 GHz (from 1375 to 2375 MHz).

A Tetronix TDS 684A oscilloscope was used as the ADC to collect the digitized data. The scope operated at 2.5 GHz and had 8 bit output. The 8 bit outputs were converted into 2 bits through a software program. These 2

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bit data were processed through a one bit kernel function simulated in a computer program. The maximum number of output bits of the adders were limited to 7 to reduce hardware when it is fabricated on a chip. The highest two frequencies to cross certain thresholds will be declared as the desired signals.

First, no signal was applied to the input, the program was run to detect false alarm. For 10,000 runs 7 false signals were recorded. The result can be listed in Table 1.

Table 1. Result of false alarm

	False alarm rate(%)
no input signal	0.007

Second, one signal with random frequency was applied to the input of the set-up with amplitude ranges from -70 to 10 dBm in 10 dB steps. At each power level, 100 runs were performed. If the output frequency is within ±6 MHz of the input signal, it is considered as the correct answer. The results are shown in Table 2. The frequency reading was always correct. However, some false alarm was recorded as a second signal.

Table 2. Result from one signal

	Found Actual Signal (%)	Found False Signal (%)
Single Input Signal	100.0	0.9

When the input signal amplitude was at -75 dBm, the receiver detected the input signal 88% of the time and generated one false alarm.

Finally, two simultaneous signals were applied to the input. The two signal were random in frequency, but their amplitude must be very close, otherwise the receiver will miss the weaker signal. The minimum frequency separation was 20 MHz and the maximum amplitude separation was set to 5 dB. If the two signals are separated by more than 5 dB, the receiver will read the strong signal only. One signal amplitude changed from 10 to -70 dBm. At each of these power levels the second signal changed from 0 to -5dB with respect to the first one. At each combination of power levels 100 runs were taken. The results are shown in Table 3. The receiver usually read both frequencies correctly when the two signals are close in amplitude.

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Table 3. Result from two signals

Magnitude of 2nd Signal vs. 1st Signal (dB)	Found 1st Signal (%)	Found 2nd Signal (%)	Found Both Signals (%)	Found Neither Signal (%)	Found False Signal (%)
0	69.1	73.1	42.3	0.11	1.0
-1	82.6	58.1	40.9	0.22	1.3
-2	92.3	38.6	30.4	0.11	2.0
-3	94.9	26.7	21.2	0.00	1.7
-4	97.8	17.9	15.9	0.22	1.3
-5	99.2	11.7	15.9	0.00	0.89
average				0.11	1.37

Sometimes the receiver misses both signals, because neither signal crosses the threshold. Sometimes, the receiver read a spurious signal rather than the true signal. In this table each value was obtained from 900 runs. The overall performance of the receiver can be considered as with 99.89% (100%-0.11%) probability of detection and 1.37% of false data.

IV. COMPARISON OF MONOBIT RECEIVER WITH A CONVENTIONAL DIGTIAL RECEIVER

The performance the monobit receiver can only be measured, because the front end of the receiver is nonlinear and the 2 bit ADC is also highly nonlinear. The performance of a conventional digital receiver can be predicted from the ADC performance and the capability FFT. Assume that the ADC has 8 bits and operates at 3 GHz. The performance of the two receivers is listed in Table 4.

Table 4. Comparison of conventional digital and monobit receivers

	Digital receiver	Monobit receiver
Bandwidth (GHz)	1	1
Number of FFT points	32	256
Single Signal dynamic range (dB)	55	80
2 signal spur free dynamic range (dB)	50	80
2 signal instantaneous dynamic range (dB)	50	5
Amplitude measurement	yes	no
Number of input signals	4*	2**
minimum pulse width (ns)	100	100

***** is not theoretically limited ** theoretically limited

V. SUMMARY

From the limited data collected, it appears that the monobit receiver can process two simultaneous signals. The results should be improved through some logic circuit design changes. A chip can be designed to take digitized data as input and perform the monobit FFT. The chip can also include the frequency selection logic. The overall performance can only be obtained when the receiver is built in hardware.

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